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FREESCALE SEMICONDUCTOR, INC.

**UNITED STATES DISTRICT COURT**  
**NORTHERN DISTRICT OF CALIFORNIA**  
**OAKLAND DIVISION**

MEDIATEK INC.,

Plaintiff,

v.

FREESCALE SEMICONDUCTOR, INC.,

Defendant.

Case No. 4:11-cv-05341 YGR

**FREESCALE'S 35 U.S.C. § 282  
DISCLOSURE**

1 Pursuant to 35 U.S.C. § 282, Defendant Freescale Semiconductor, Inc. (Freescale) makes  
2 the following disclosures to Plaintiff MediaTek Inc. (MediaTek). Freescale gives notice of each  
3 patent and publication that may be “relied upon as anticipation of [a] patent-in-suit or . . . as  
4 showing the state of the art,” and the names and addresses of each person “who may be relied  
5 upon as the prior inventor or as having prior knowledge of or as having previously used or offered  
6 for sale the invention of [a] patent-in-suit.”

7 **U.S. Patents**

- 8 1. U.S. Patent No. 6,889,331 (Soerensen et al.) issued on 5/3/2005– “Dynamic voltage  
9 control method and apparatus”
- 10 2. U.S. Patent No. 5,606,293 (Matsui et al.) issued on 2/25/1997 – “Clock Generator for  
11 microcomputer having reduced start-up time”
- 12 3. U.S. Patent No. 5,774,701 (Matsui et al.) issued on 6/30/1998 – “Microprocessor  
13 operating at high and low clock frequencies”
- 14 4. U.S. Patent No. 6,005,904 (Knapp et al.) issued on 12/21/1999 – “Phase-locked loop with  
15 protected output during instances when the phase-locked loop is unlocked”
- 16 5. U.S. Patent No. 6,118,306 (Orton et al.) issued on 9/12/2000 – “Changing clock  
17 frequency”
- 18 6. U.S. Patent No. 6,425,086 (Clark et al.) issued on 7/23/2002 – “Method and apparatus for  
19 dynamic power control of a low power processor”
- 20 7. U.S. Patent No. 5,623,234 (Shaik et al.) issued on 4/22/1997 – “Clock system”
- 21 8. U.S. Patent No. 6,625,740 (Datar et al.) issued on 9/23/2003 – “Dynamically activating  
22 and deactivating selected circuit blocks of a data processing integrated circuit during  
23 execution of instructions according to power code bits appended to selected instructions”
- 24 9. U.S. Patent No. 6,311,287 (Dischler et al.) issued on 10/30/2001 – “Variable frequency  
25 clock control for microprocessor-based computer systems”
- 26 10. U.S. Patent No. 7,100,061 (Halepete et al.) issued on 8/29/2006 – “Adaptive power  
27 control”
- 28 11. U.S. Patent No. 6,088,753 (Sheafor et al.) issued on 7/11/2000 – “Bus arrangements for

- 1 interconnection of discrete and/or integrated modules in a digital system and associated  
2 method”
- 3 12. U.S. Patent No. 6,311,244 (Sheafor et al.) issued on 10/30/2001 – “Priority allocation in a  
4 bus interconnected discrete and/or integrated digital multi-module system”
- 5 13. U.S. Patent No. 5,483,642 (Okazawa et al.) issued on 1/9/1996 – “Bus system for use with  
6 information processing apparatus”
- 7 14. U.S. Patent No. 4,845,663 (Brown et al.) issued on 7/4/1989 – “Image processor with free  
8 flow pipeline bus”
- 9 15. U.S. Patent No. 5,289,585 (Kock et al.) issued on 2/22/1994 – “Multiprocessor system  
10 having a system bus for the coupling of several processing units with appertaining private  
11 cache memories and a common main memory”
- 12 16. U.S. Patent No. 5,481,677 (Kai et al.) issued on 1/2/1996 – “Data transfer system in which  
13 data is transferred to or from a data memory during an instruction fetch cycle”
- 14 17. U.S. Patent No. 5,490,253 (Laha et al.) issued on 2/6/1996 – “Multiprocessor system  
15 using odd/even data buses with a timeshared address bus”
- 16 18. U.S. Patent No. 5,500,949 (Saito) issued on 3/19/1996 – “Microprocessor system for  
17 inhibiting access to memory by checking specific address and specific codes”
- 18 19. U.S. Patent No. 5,590,124 (Robins) issued on 12/31/1996 – “Link and discovery protocol  
19 for a ring interconnect architecture”
- 20 20. U.S. Patent No. 5,666,551 (Fenwick et al.) issued on 9/9/1997 – “Distributed data bus  
21 sequencing for a system bus with separate address and data bus protocols”
- 22 21. U.S. Patent No. 5,751,999 (Suzuki) issued on 5/12/1998 – “Processor and data memory  
23 for outputting and receiving data on different buses for storage in the same location”
- 24 22. U.S. Patent No. 5,768,550 (Dean et al.) issued on 6/16/1998 – “Bus interface logic  
25 system”
- 26 23. U.S. Patent No. 5,850,521 (Morganti et al.) issued on 12/15/1998 – “Apparatus and  
27 method for interprocessor communication”
- 28 24. U.S. Patent No. 5,019,962 (Funabashi et al.) issued on 5/28/1991 – “Direct memory

- 1 access controller for a multi-microcomputer system”
- 2 25. U.S. Patent 5,584,010 (Kawai et al.) issued on 12/10/1996 – “Direct memory access
- 3 control device and method in a multiprocessor system accessing local and shared
- 4 memory”
- 5 26. U.S. Patent No. 6,738,845 (Hadwiger et al.) issued on 5/18/2004 – “Bus architecture and
- 6 shared bus arbitration method for a communication device”
- 7 27. U.S. Patent No. 4,276,594 (Morley) issued on 6/30/1981 – “Digital computer with multi-
- 8 processor capability utilizing intelligent composite memory and input/output modules and
- 9 method for performing the same”
- 10 28. U.S. Patent No. 4,639,910 (Toegel et al.) issued on 1/27/1987 – “Apparatus for
- 11 establishing communication paths”
- 12 29. U.S. Patent No. 4,698,753 (Hubbins et al.) issued on 10/6/1987 – “Multiprocessor
- 13 interface device”
- 14 30. U.S. Patent No. 5,278,974 (Lemmon et al.) issued on 1/11/1994 – “Method and apparatus
- 15 for the dynamic adjustment of data transfer timing to equalize the bandwidths of two
- 16 buses in a computer system having different bandwidths”
- 17 31. U.S. Patent No. 5,467,295 (Young et al.) issued on 11/14/1995 – “Bus arbitration with
- 18 master unit controlling bus and locking a slave unit that can relinquish bus for other
- 19 masters while maintaining lock on slave unit”
- 20 32. U.S. Patent No. 5,539,882 (Gopal et al.) issued on 7/23/1996 – “Method and system for an
- 21 efficient multiple access polling protocol for interactive communication”
- 22 33. U.S. Patent No. 5,627,976 (McFarland et al.) issued on 5/6/1997 – “Crossing transfers for
- 23 maximizing the effective bandwidth in a dual-bus architecture”
- 24 34. U.S. Patent No. 5,634,004 (Gopinath et al.) issued on 5/27/1997 – “Directly
- 25 programmable distribution element”
- 26 35. U.S. Patent No. 5,649,209 (Umetsu et al.) issued on 7/15/1997 – “Bus coupling
- 27 information processing system for multiple access to system bus”
- 28 36. U.S. Patent No. 5,649,233 (Chen) issued on 7/15/1997 – “Apparatus for flexibly selecting

- 1 primary and secondary connectors and master and slave cascaded disk drives of an ide  
2 interface”
- 3 37. U.S. Patent No. 5,734,848 (Gates et al.) issued on 3/31/1998 – “Method and apparatus for  
4 transferring data in a controller having centralized memory”
- 5 38. U.S. Patent No. 5,754,780 (Asakawa et al) issued on 5/19/1998 – “Apparatus and method  
6 for performing serial communication between master and slave devices”
- 7 39. U.S. Patent No. 5,909,559 (So) issued on 6/1/1999 – “Bus bridge device including data  
8 bus of first width for a first processor, memory controller, arbiter circuit and second  
9 processor having a different second data width”
- 10 40. U.S. Patent No. 5,931,931 (Nguyen) issued on 8/3/1999 – “Method for bus arbitration in a  
11 multiprocessor system”
- 12 41. U.S. Patent No. 5,987,549 (Hagersten et al.) issued on 11/16/1999 – “Method and  
13 apparatus providing short latency round-robin arbitration for access to a shared resource”
- 14 42. U.S. Patent No. 6,006,303 (Barnaby et al.) issued on 12/21/1999 – “Priority encoding  
15 and decoding for memory architecture”
- 16 43. U.S. Patent No. 6,026,461 (Baxter et al.) issued on 2/15/2000 – “Bus arbitration system  
17 for multiprocessor architecture”
- 18 44. U.S. Patent No. 6,038,630 (Foster et al.) issued on 3/14/2000 – “Shared access control  
19 device for integrated system with multiple functional units accessing external structures  
20 over multiple data buses”
- 21 45. U.S. Patent No. 6,047,349 (Klein) issued on 4/4/2000 – “System for communicating  
22 through a computer system bus bridge”
- 23 46. U.S. Patent No. 6,061,361 (An et al.) issued on 5/9/2000 – “Time multiplexed scheme for  
24 deadlock resolution in distributed arbitration”
- 25 47. U.S. Patent No. 6,070,205 (Kato et al.) issued on 5/30/2000 – “High-speed processor  
26 system having bus arbitration mechanism”
- 27 48. U.S. Patent No. 6,223,230 (Garnett et al.) issued on 4/24/2001 – “Direct memory access in  
28 a bridge for a multi-processor system”

- 1 49. U.S. Patent No. 6,347,294 (Booker et al.) issued on 2/12/2002 – “Upgradeable highly  
2 integrated embedded CPU system”
- 3 50. U.S. Patent No. 6,363,453 (Esposito et al.) issued on 3/26/2002 – “Parallel processor with  
4 redundancy of processor pairs”
- 5 51. U.S. Patent No. 6,389,493 (Barkley et al.) issued on 5/14/2002 – “System and method for  
6 dynamically allocating bandwidth to a plurality of slave cards coupled to a bus”
- 7 52. U.S. Patent No. 6,496,740 (Robertson et al.) issued on 12/17/2002 – “Transfer controller  
8 with hub and ports architecture”
- 9 53. U.S. Patent No. 6,496,890 (Azevedo et al. issued on 12/17/2002) – “Bus hang prevention  
10 and recovery for data communication systems employing a shared bus interface with  
11 multiple bus masters”
- 12 54. U.S. Patent No. 6,519,666 (Azevedo et al.) issued on 2/11/2003 – “Arbitration scheme for  
13 optimal performance”
- 14 55. U.S. Patent No. 6,671,761 (Kim) issued on 12/30/2003 – Bus system”
- 15 56. U.S. Patent No. 5,546,547 (Bowes et al.) issued on 8/13/1996 – “Memory bus arbiter for a  
16 computer system having a DSP co-processor”
- 17 57. U.S. Patent No. 5,828,856 (Bowes et al.) issued on 10/27/1998 – “Dual bus concurrent  
18 multi-channel direct memory access controller and method”

#### 19 **Foreign Patents/Published Applications**

- 20 1. European Patent Application EP 0 632 360 A1 (Weiser et al.) published on 1/4/1995 –  
21 “Reducing computer power consumption by dynamic voltage and frequency variation”
- 22 2. European Patent Application EP 0 895 358 A2 (Hardesty et al.) published on 2/3/1999 –  
23 “Fast start-up processor clock generation method and system”
- 24 3. European Patent Application EP 0 978 781 A2 (Nicol et al.) published on 2/9/2000 –  
25 “Power reduction in a multiprocessor digital signal processor”
- 26 4. European Patent Application EP 0 991 191 A2 (Houston) published on 4/5/2000 –  
27 “System and method for reducing power dissipation in a circuit”
- 28 5. European Patent Publication EP 0 458 516 B1 (Laha et al.) published on 11/5/1997 –

- 1 “Memory access bus arrangement”
- 2 6. European Patent Publication EP 0 460 853 B1 (Kass et al.) published on 3/3/1999 –
- 3 “Memory system”
- 4 7. European Patent Publication EP 0 426 413 B1 (Jansen et al.) published on 5/7/1997 –
- 5 “Multiprocessor arbitration in single processor arbitration schemes”
- 6 8. European Patent Application EP 0 702 307 A1 (Leung) published on 3/20/1996 –
- 7 “Multibus dynamic arbiter”
- 8 9. European Patent Application EP 0 924 623 A2 (Reif et al.) published on 6/23/1999 –
- 9 “Computer system including arbitration mechanism allowing multiple bus masters to
- 10 access a graphics bus”
- 11 10. PCT Patent Application WO 99/26155 (Knight et al.) published on 5/27/1999 –
- 12 “Peripheral servicing”

### 13 **Publications**

- 14 1. Allen, Simplified Dynamic Voltage Control Intellectual Property Disclosure (August 26,
- 15 2001), 1-5.
- 16 2. McFarling, Turney and Mudge, VLSI Crossbar Design Version Two (February 1982), 1-
- 17 18.
- 18 3. Chambers, The Ten Commandments of Excellent Design (1997), 1- 20.
- 19 4. Motorola, MC88410 Secondary Cache Controller User’s Manual (1992), 1-1 - 6-28.
- 20 5. Frank and Lyle, SBus Specification B.0 (1990), 1-186.
- 21 6. ICAP, Supplemental to High Speed Embedded Interconnects Patent Offering Package
- 22 Covering Intellectual Property Assets of Vitesse Semiconductor Corporation: ARM 11 A
- 23 Survey of Product Implementation (n.d.), 1-41.
- 24 7. Appendix 1: Standard Product Designs Impacted by the Selected Interconnect Patent
- 25 (n.d.), MTK-00030387 – MTK-00030466.
- 26 8. ICAP, Patent Offering Package Covering Intellectual Property Assets of Vitesse
- 27 Semiconductor Corporation: High Speed Embedded Interconnects Patents and Broadcom
- 28 (n.d.), MTK-00030501 – MTK-00030610.

- 1 9. ICAP, Vitesse Semiconductor Patent Offering (n.d.), MTK-00030681 – MTK-00030746.
- 2 10. ICAP, Patent Offering Package Covering Intellectual Property Assets of Vitesse
- 3 Semiconductor Corporation: High Speed Embedded Interconnects (n.d.), MTK-
- 4 00030747- MTK-00030816.
- 5 11. Sorensen, Analog Devices: MSP430 Hercules Bus architecture definition Architecture
- 6 Specification (February 27, 1998), 1-10.
- 7 12. Bhuyan, Yang and Agrawal, Performance of Multiprocessor Interconnection Networks
- 8 (February 1989), 25-37.
- 9 13. Vitesse, Design Manual: IQ2000 Family of Network Processors (2000), VIT000106-
- 10 VIT000803.
- 11 14. Vitesse, Design Manual: IQ2000 Family of Network Processors (2000), VIT000804-
- 12 VIT001527.
- 13 15. Carr, Fusion Memory Architecture Specification (May 12, 1997), 1-64.
- 14 16. Sitera, PRISM Design Manual (1998), VIT001622-VIT002289.
- 15 17. Vitesse, Application Note: Basic Design Using the IQ200 Network Processor (2000), 1-
- 16 20.
- 17 18. Vitesse, A Day In The Life Of A Packet: IQ2000 Network Processor Theory of Operation
- 18 Overview (2000), 1-20.
- 19 19. Osborn, IQ2200 Training-Vitesse ANP Overview: NPY Product Training (July 16, 1996),
- 20 VIT002330-VIT002404.
- 21 20. Vitesse, Day in the Life of a Packet: Detailed Multicast Egress Flow (July 16, 1996),
- 22 VIT002405-VIT002479.
- 23 21. Vitesse, CSIX Upper Layers (July 16, 1996), VIT002480-VIT002550.
- 24 22. Chipworks, MediaTek Various Patent analysis on ARM Processors Bus Architecture
- 25 (May 27, 2009), MTK-00034333-MTK-00034352.
- 26 23. AMBA, AMBA Advanced Microcontroller BUS Architecture Specification (April 1997),
- 27 1-1 – 6-20.
- 28 24. ARM, AMBA Specification (May 13, 1999), 1-1 – 3-57.



- 1 25. IBM, CoreConnect Bus Architecture (n.d.), 1.
- 2 26. The CoreConnect Bus Architecture (n.d.), 1-8.
- 3 27. ARM, AMBA AXI Protocol (June 16, 2003)
- 4 28. IBM, PLB Crossbar Arbiter Core User's Manual (July 2002), 1-7.

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25 To the extent not cited above, Freescale incorporates by reference any patents,  
26 publications, and things cited on the face, in the specification, or in the prosecution history of any  
27 of the patents-in-suit (including foreign prosecution histories and search reports) and any patents,  
28 publications, things, or persons identified in any interrogatory responses, depositions, expert

1 reports, Rule 26(a) disclosures, Patent Rule 3-3 Invalidity Contentions, or made known to  
2 MediaTek through discovery or otherwise.

3  
4 Dated: January 24, 2014

Respectfully Submitted,

5  
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19 Attorneys for Defendant-Counterclaimant  
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21 **ATTESTATION OF E-FILED SIGNATURE**

22 I, Rudy Y. Kim, am the ECF User whose ID and password are being used to file  
23 Freescale's 35 U.S.C. § 282 Disclosure. In compliance with General Order 45, X.B., I hereby  
24 attest that Joshua A. Hartman has concurred in this filing.

25 Dated: January 24, 2013

/s/ Rudy Y. Kim  
Rudy Y. Kim